UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/981,646	10/16/2001	Anthony Debling	S1022/8762	7546

23628 7590 11/18/2004

WOLF GREENFIELD & SACKS, PC
FEDERAL RESERVE PLAZA
600 ATLANTIC AVENUE
BOSTON, MA 02210-2211

EXAMINER	
MCCARTHY, CHRISTOPHER S	
ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/981,646	DEBLING, ANTHONY
	Examiner	Art Unit
	Christopher S. McCarthy	2113

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☒ Claim(s) *14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Response to Arguments*.

DETAILED ACTION

1. Claims 1-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Swoboda U.S. Patent Application Publication US2002/0059541, as cited in prior office action, which was mailed on 7/22/2004.

2. Claims 14-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, as cited in prior office action, which was mailed on 7/22/2004.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Swoboda U.S. Patent Application Publication US2002/0059541.

As per claim 1, Swoboda teaches an integrated circuit chip comprising an embedded digital processor (paragraph 0031, 0069) and an on-chip emulation device coupled to said digital

processor, said emulation device being operable to control said digital processor and to collect information about the operation of said digital processor (paragraph 0061, 0055), the on-chip emulation device having a communication port for off-chip communication (paragraph 0061, 0038, 0080), the chip further comprising an on-chip interface having a first port connected to said communication port of said on-chip emulation device (paragraph 0080) and a second port for connection to a non-proprietary bus (paragraph 0080) wherein said interface is operable to convert between a format suitable for said on-chip emulation device and a format suitable for said non-proprietary bus (paragraph0080, 0064, 0066).t

As per claim 2, Swoboda teaches the integrated circuit chip of claim 1 having plural embedded digital processors, each having a respective associated on-chip emulation device and a respective said on-chip interface, said integrated circuit chip further including said non-proprietary bus, and a bus connection port connected on said chip via said non-proprietary bus to the second port of each said interface (paragraph 0082).

As per claim 3, Swoboda teaches the integrated circuit chip of claim 1 wherein said non-proprietary bus is a universal serial bus (paragraph 0066).

As per claim 4, Swoboda teaches the integrated circuit chip of claim 3 wherein said bus connection port is a universal serial bus hub (paragraph0066, 0039, wherein, it is inherent with multiple connections, which could be multiple USB connections, that a hub be used to control the co-existing connections).

As per claim 5, Swoboda teaches the integrated circuit chip of claim 1 wherein said non-proprietary bus is a bus complying with IEEE standard 1394 (paragraph 0067).

As per claim 6, Swoboda teaches the integrated circuit chip of claim 1 wherein the or each digital processor further comprises JTAG circuitry connected to said bus (paragraph 0062).

As per claim 7, Swoboda teaches the integrated circuit chip of claim 6 wherein said JTAG circuitry has a further off-chip connection (paragraph 0069).

As per claim 8, Swoboda teaches a method of communicating between a remote device and a digital processor (paragraph 0031, 0060, 0038), said digital processor being on an integrated circuit chip (paragraph 0069), said chip having on-chip emulation circuitry for monitoring and controlling the digital processor in response to signals from a said remote device (paragraph 0081), said chip further comprising interface circuitry disposed between a port of said on-chip emulation circuitry and a communication port for said signals (paragraph 0080, wherein, the circuitry is inherent in the port driver interface), wherein said port is adapted to receive a non-proprietary bus and wherein said non-proprietary bus is adapted to convey signals having a predetermined protocol (paragraph 0080, 0064, 0066, wherein, the protocol is inherent in the proper communication of a USB connection), the method comprising: connecting said non-proprietary bus to said port and to a said remote device (paragraph 0080); receiving said signals from said remote device over said non-proprietary bus in said non-proprietary protocol at said communication port and transferring said signals to said interface circuitry on-chip (paragraph 0080, 0064, 0066); in said interface circuitry, converting said signals into a form suitable for said on-chip emulation circuitry, and transferring said converted signals to said on-chip emulation circuitry whereby said on-chip emulation circuitry responds to said converted signals to monitor and control said digital processor (paragraph 0080, 0064, 0066, 0039, 0060).

As per claim 9, Swoboda teaches a method of debugging a digital processor using a host computer, said digital processor being on an integrated circuit chip (paragraph 0031, 0060, 0038, 0069), said chip having on-chip emulation circuitry for monitoring and controlling the digital processor in response to signals from said host computer (paragraph 0081, 0080), said chip further comprising interface circuitry disposed between a port of said on-chip emulation circuitry and a communication port for said signals (paragraph 0080), wherein said port is adapted to receive a non-proprietary bus and wherein said non-proprietary bus is adapted to convey signals having a predetermined protocol (paragraph 0080, 0064, 0066), the method comprising: connecting said non-proprietary bus to said port and to a said host computer (paragraph 0080, 0064, 0066); generating said signals in said host computer (paragraph 0039, 0060); receiving said signals from said host computer over said non-proprietary bus in said non-proprietary protocol at said communication port and transferring said signals to said interface circuitry on-chip (paragraph 0039, 0060, 0066, 0064); in said interface circuitry, converting said signals into a form suitable for said on-chip emulation circuitry, and transferring said converted signals to said on-chip emulation circuitry whereby said on-chip emulation circuitry responds to said converted signals to monitor and control said digital processor (0081, 0039, 0060, 0064, 0066).

As per claim 10, Swoboda teaches the method of claim 8 wherein said chip further comprises peripheral circuitry, and said on-chip emulation circuitry is linked to said peripheral circuitry for control and monitoring thereof (paragraph 0069).

As per claim 11, Swoboda teaches the method of claim 8 wherein said non-proprietary bus is a universal serial bus and said predetermined protocol is a universal serial bus protocol

(paragraph 0064, 0066, wherein, the protocol of USB is inherent in the use of the USB connection).

As per claim 12, Swoboda teaches the method of claim 11 wherein said integrated circuit chip further comprises JTAG circuitry connected to said interface circuitry, the method further comprising supplying test signals over said universal serial bus to said interface circuitry; in said interface circuitry converting said test signals into JTAG protocol form; and supplying said JTAG protocol signals to said JTAG circuitry whereby said JTAG circuitry implements boundary test functions of said chip (paragraph 0080 – 0082).

As per claim 13, Swoboda teaches the method of claim 12 further comprising causing said on-chip emulation circuitry to determine data illustrative of the behaviour of said chip said signals comprise interrogating signals for said on-chip emulation circuitry, whereby said on-chip emulation circuitry derives information from said data to said interface; in said interface, converting said information into universal serial bus protocol; and transmitting said information in universal serial bus protocol over said universal serial bus to said host (paragraph 0080–0082).

Allowable Subject Matter

4. Claims 14-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments filed 10/25/2004 have been fully considered but they are not persuasive.

Applicant has argued that Swoboda does not teach or suggest an integrated circuit chip comprising an embedded digital processor and an on-chip emulation device coupled to said digital processor. The examiner respectfully disagrees. The applicant is correct in his assertion that Swoboda utilizes an off-chip emulator controller, but as Swoboda clearly teaches in paragraph 0055, the emulator, as a whole, consists of four components. The last component taught is an "on-chip debug facility" (paragraph 0059). Since this debug facility is clearly on-chip and is an inclusive component of the emulator device, then an integral component of the emulator is on-chip and fulfills the limitation of an on-chip emulator. Therefore, all applicable rejected claims stand.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher S. McCarthy whose telephone number is (571)272-3651. The examiner can normally be reached on M-F, 9 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

csm
11/12/2004

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100